IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Paul L. Master, et al.	)	Examiner: Idriss N. Alrobaye
	)	Group Art Unit: 2183
Appl. No.: 09/997,530	)	
Filed: November 30, 2001	)	
For: APPARATUS, SYSTEM AND METHOD FOR CONFIGURATION OF ADAPTIVE INTEGRATED CIRCUITRY HAVING FIXED, APPLICATION SPECIFIC COMPUTATIONAL ELEMENTS	)	

Proposed **RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT and AMENDMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following Amendments and Remarks are made in response to the Notice Of Non-Compliant Amendment mailed on February 20, 2009. A Petition for an extension of time under 37 C.F.R. § 1.136(a) are also being submitted herewith. Reexamination and reconsideration of the application in light of the following Amendments and Remarks are respectfully requested.

Amendments to the Claims begins on page 2 of this paper.

Remarks begin on page 31 of this paper.

Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of claims in the application where added material is shown in underlined type, deleted material is shown in ~~strikeout type~~ or within double brackets:

Listing of Claims:

Claims 1-181 (Canceled)

182. (New) A system for adaptive configuration, the system comprising:

configuration information including a first configuration information and a second configuration information;

a memory adapted to store the configuration information;

a first plurality of heterogeneous computational elements;

a second plurality of heterogeneous computational elements;

an interconnection network coupled to the memory, the interconnection network including:

a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together; and

a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together;

a configurable basic computational unit including the first plurality of heterogeneous computational elements and the first interconnection network, the first interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function; and

a configurable complex computational unit including the second plurality of heterogeneous computational elements and the second interconnection network, the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function.

183. (New) The system of claim 182, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

184. (New) The system of claim 182, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information.

185. (New) The system of claim 182, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information.

186. (New) The system of claim 182, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface.

187. (New) The system of claim 182, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits.

188. (New) The system of claim 182, wherein the system is embodied within an integrated circuit.

189. (New) The system of claim 182, wherein the computational units are organized in a computing matrix and the computing matrix is coupled to a matrix interconnection network.

190. (New) The system of claim 189, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrixes, each configurable computing matrix having a plurality of computational units.

191. (New) The system of claim 182, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

192. (New) The system of claim 189, wherein a first configured function of the configurable computing matrix is as a controller.

193. (New) The system of claim 190, wherein a first configured function of the computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrixes.

194. (New) The system of claim 192, wherein the controller is a RISC controller.

195. (New) The system of claim 182, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

196. (New) The system of claim 195, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

197. (New) The system of claim 182, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

198. (New) The system of claim 182, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

199. (New) The system of claim 182, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

200. (New) The system of claim 199, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

201. (New) The system of claim 200, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

202. (New) The system of claim 182, wherein basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

203. (New) The system of claim 202, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

204. (New) The system of claim 203, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

205. (New) The system of claim 182, wherein the basic computational function includes one of a group of linear operation, non-linear operation, finite state machine computing, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

206. (New) The system of claim 205, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

207. (New) The system of claim 206, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

208. (New) The system of claim 207, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

209. (New) The system of claim 208, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

210. (New) The system of claim 182, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex processing unit, the third interconnection network sending the configuration information to the units.

211. (New) The system of claim 210, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

212. (New) The system of claim 182, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements.

213. (New) The system of claim 212, wherein the configuration information includes control signals to control the multiplexers.

214. (New) The system of claim 182, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

215. (New) A system for adaptive configuration, the system comprising:

configuration information including a first configuration information and a second configuration information;

a memory adapted to store the configuration information;

a first plurality of heterogeneous computational elements;

a second plurality of heterogeneous computational elements;

an interconnection network coupled to the memory, the interconnection network comprising:

a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together;

a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together;

a first computational unit having a configurable basic architecture including the first plurality of heterogeneous computational elements and the first interconnection network, the first interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function; and

a second computational unit having a configurable complex processing architecture including the second plurality of heterogeneous computational elements and the second interconnection network, the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function.

216. (New) The system of claim 215, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

217. (New) The system of claim 215, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information.

218. (New) The system of claim 215, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information.

219. (New) The system of claim 215, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface.

220. (New) The system of claim 215, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits.

221. (New) The system of claim 215, wherein the system is embodied within an integrated circuit.

222. (New) The system of claim 215, wherein the computational units are organized in a configurable computing matrix and the computing matrix is coupled to a matrix interconnection network.

223. (New) The system of claim 222, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrixes, each configurable computing matrix having a plurality of computational units.

224. (New) The system of claim 222, wherein a first configured function of the configurable computing matrix is as a controller.

225. (New) The system of claim 223, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrixes.

226. (New) The system of claim 224, wherein the controller is a RISC controller.

227. (New) The system of claim 215, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

228. (New) The system of claim 227, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

229. (New) The system of claim 215, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

230. (New) The system of claim 215, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

231. (New) The system of claim 215, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

232. (New) The system of claim 231, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

233. (New) The system of claim 232, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

234. (New) The system of claim 215, wherein basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

235. (New) The system of claim 234, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

236. (New) The system of claim 235, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

237. (New) The system of claim 215, wherein the basic computational function includes one of a group of linear operation, non-linear operation, finite state machine computing, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

238. (New) The system of claim 237, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

239. (New) The system of claim 238, wherein the basic computational function comprises bit level manipulation; and

wherein the complex computational function comprises word level manipulation.

240. (New) The system of claim 239, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

241. (New) The system of claim 240, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

242. (New) The system of claim 215, further comprising a third interconnection network coupled to the first computational unit and the second computational unit, the third interconnection network sending the configuration information to the computational units.

243. (New) The system of claim 242, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

244. (New) The system of claim 215, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements.

245. (New) The system of claim 244, wherein the configuration information includes control signals to control the multiplexers.

246. (New) A system for adaptive configuration, the system comprising:

configuration information including a first configuration information and a second configuration information;

a memory adapted to store the configuration information;

a first plurality of heterogeneous computational elements;

a second plurality of heterogeneous computational elements;

an interconnection network coupled to the memory, the interconnection network comprising:

a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together;

a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together;

a first configurable basic computational logic unit including the first plurality of heterogeneous computational elements and the first interconnection network for forming a first configurable architecture, the first computational interconnection network configuring interconnections between the first plurality of heterogeneous computational elements in response to the first configuration information to perform a basic computational function; and

a second configurable complex processing unit including the second plurality of heterogeneous computational elements and the second interconnection network for forming a second configurable architecture, the second interconnection network configuring interconnections between the second plurality of heterogeneous computational elements in response to the second configuration information to perform a complex processing function.

247. (New) The system of claim 246, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

248. (New) The system of claim 246, wherein the first plurality of heterogeneous computational elements are configured to generate a request for the second configuration information.

249. (New) The system of claim 246, wherein the memory comprises a third plurality of heterogeneous computational elements configured to perform a memory function in response to the configuration information.

250. (New) The system of claim 246, wherein the configuration information is transferred to the system from a machine-readable medium or through a wireless interface.

251. (New) The system of claim 246, wherein the configuration information is embodied as a plurality of discrete information data packets or as a stream of information data bits.

252. (New) The system of claim 246, wherein the system is embodied within an integrated circuit.

253. (New) The system of claim 246, wherein the logic unit and processing unit are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

254. (New) The system of claim 253, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrixes, each configurable computing matrix having a plurality of logic and processing units.

255. (New) The system of claim 246, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

256. (New) The system of claim 253, wherein a first configured function of the configurable computing matrix is as a controller.

257. (New) The system of claim 254, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrixes.

258. (New) The system of claim 256, wherein the controller is a RISC controller.

259. (New) The system of claim 246, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

260. (New) The system of claim 259, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

261. (New) The system of claim 246, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

262. (New) The system of claim 246, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

263. (New) The system of claim 246, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

264. (New) The system of claim 263, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

265. (New) The system of claim 264, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

266. (New) The system of claim 246, wherein basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

267. (New) The system of claim 266, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

268. (New) The system of claim 267, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

269. (New) The system of claim 246, wherein the basic computational function includes one of a group of linear operation, non-linear operation, finite state machine computing, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

270. (New) The system of claim 269, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

271. (New) The system of claim 270, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

272. (New) The system of claim 271, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

273. (New) The system of claim 272, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

274. (New) The system of claim 246, further comprising a third interconnection network coupled to the first configurable basic computational unit and the second configurable complex processing unit, the third interconnection network sending the configuration information to the units.

275. (New) The system of claim 274, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

276. (New) The system of claim 246, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements.

277. (New) The system of claim 276, wherein the configuration information includes control signals to control the multiplexers.

278. (New) The system of claim 246, wherein the first interconnection network provides a third configuration information to reconfigure the first configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

279. (New) A method for adaptive configuration of an integrated circuit, the integrated circuit having a first plurality of heterogeneous computational elements, a second plurality of heterogeneous computational elements, and an interconnection network coupled to the memory, the interconnection network having a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together, the method comprising:

receiving configuration information;

storing the configuration information in a memory; and

in response to the configuration information:

configuring interconnections between the first plurality of heterogeneous computational elements via the first interconnection network to provide a configurable basic computational unit to perform a basic computational function; and

configuring interconnections between the second plurality of heterogeneous computational elements via the second interconnection network to provide a configurable complex computational unit to perform a complex processing function.

280. (New) The method of claim 279, further comprising requesting authorization to receive the configuration information.

281. (New) The method of claim 279, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

282. (New) The method of claim 279, wherein the configuration information is received from a machine-readable medium or via a wireless interface.

283. (New) The method of claim 279, wherein the computational units are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

284. (New) The method of claim 283, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrixes, each configurable computing matrix having a plurality of computational units.

285. (New) The method of claim 279, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

286. (New) The method of claim 283, wherein a first configured function of the configurable computing matrix is as a controller.

287. (New) The method of claim 284, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrixes.

288. (New) The method of claim 286, wherein the controller is a RISC controller.

289. (New) The method of claim 279, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

290. (New) The method of claim 283, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

291. (New) The method of claim 279, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

292. (New) The method of claim 279, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

293. (New) The method of claim 279, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

294. (New) The method of claim 293, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

295. (New) The method of claim 294, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

296. (New) The method of claim 279, wherein basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

297. (New) The method of claim 296, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

298. (New) The method of claim 297, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

299. (New) The method of claim 279, wherein the basic computational function includes one of a group of linear operation, non-linear operation, finite state machine computing, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

300. (New) The method of claim 299, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

301. (New) The method of claim 300, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

302. (New) The method of claim 301, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

303. (New) The method of claim 302, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

304. (New) The method of claim 279, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex computational unit, the third interconnection network sending the configuration information to the units.

305. (New) The method of claim 304, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

306. (New) The method of claim 279, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements.

307. (New) The method of claim 306, wherein the configuration information includes control signals to control the multiplexers.

308. (New) The method of claim 279, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

309. (New) A method for adaptive configuration of an integrated circuit, the integrated circuit having a first plurality of heterogeneous computational elements, a second plurality of heterogeneous computational elements, and an interconnection network coupled to the memory, the interconnection network having a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together, the method comprising:

configuring a first computational architecture, the configuring comprising configuring interconnections between the first plurality of heterogeneous computational elements via the first interconnection network in response to a first configuration information to provide a configurable basic computational unit to perform a basic computational function; and

configuring a second computational architecture, the configuring comprising configuring interconnections between the second plurality of heterogeneous computational elements via the

second interconnection network in response to a second configuration information to provide a configurable complex processing unit to perform a complex processing function.

310. (New) The method of claim 309, further comprising requesting authorization to receive the configuration information.

311. (New) The method of claim 309, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

312. (New) The method of claim 309, wherein the configuration information is received from a machine-readable medium or via a wireless interface.

313. (New) The method of claim 309, wherein the units are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

314. (New) The method of claim 313, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrixes, each configurable computing matrix having a plurality of computational units.

315. (New) The method of claim 309, wherein the first computational architecture is a basic computational architecture; and

wherein the second computational architecture is a complex processing architecture.

316. (New) The method of claim 313, wherein a first configured function of the configurable computing matrix is as a controller.

317. (New) The method of claim 314, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrixes.

318. (New) The method of claim 316, wherein the controller is a RISC controller.

319. (New) The method of claim 309, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

320. (New) The method of claim 319, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

321. (New) The method of claim 309, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

322. (New) The method of claim 309, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

323. (New) The method of claim 309, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

324. (New) The method of claim 323, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

325. (New) The method of claim 324, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

326. (New) The method of claim 309, wherein basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

327. (New) The method of claim 326, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

328. (New) The method of claim 327, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

329. (New) The method of claim 309, wherein the basic computational function includes one of a group of linear operation, non-linear operation, finite state machine computing, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

330. (New) The method of claim 329, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

331. (New) The method of claim 330, wherein the basic computational function comprises it level manipulation; and

wherein the complex processing function comprises word level manipulation.

332. (New) The method of claim 330, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

333. (New) The method of claim 332, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

334. (New) The method of claim 309, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex processing unit, the third interconnection network sending the configuration information to the units.

335. (New) The method of claim 334, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

336. (New) The method of claim 309, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements.

337. (New) The method of claim 336, wherein the configuration information includes control signals to control the multiplexers.

338. (New) The method of claim 309, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

339. (New) A method for adaptive configuration of an integrated circuit, the integrated circuit having a first plurality of heterogeneous computational elements, a second plurality of

heterogeneous computational elements, and an interconnection network coupled to the memory, the interconnection network having a first interconnection network configurably coupling the first plurality of heterogeneous computational elements together and a second interconnection network configurably coupling the second plurality of heterogeneous computational elements together, the method comprising:

transmitting configuration information;

wherein the configuration information is received;

storing the received configuration information in a memory; and

in response to the configuration information:

configuring interconnections between the first plurality of heterogeneous computational elements via the first interconnection network to provide a configurable basic computational unit to perform a basic computational function; and

configuring interconnections between the second plurality of heterogeneous computational elements via the second interconnection network to provide a configurable complex computational unit to perform a complex processing function.

340. (New) The method of claim 309, further comprising requesting authorization to receive the configuration information.

341. (New) The method of claim 339, wherein the configuration information provides a first system operating mode of the plurality of operating modes.

342. (New) The method of claim 339, wherein the configuration information is received from a machine-readable medium or via a wireless interface.

343. (New) The method of claim 339, wherein the computational units are organized in a configurable computing matrix and the configurable computing matrix is coupled to a matrix interconnection network.

344. (New) The method of claim 343, wherein the matrix interconnection network is coupled to a plurality of configurable computing matrixes, each configurable computing matrix having a plurality of computational units.

345. (New) The method of claim 339, wherein the first plurality of heterogeneous computational elements are organized as a basic computational architecture; and

wherein the second plurality of heterogeneous computational elements are organized as a complex processing architecture.

346. (New) The method of claim 343, wherein a first configured function of the configurable computing matrix is as a controller.

347. (New) The method of claim 344, wherein a first configured function of the configurable computing matrix is as a controller, and wherein the controller function includes sending configuration information via the matrix interconnection network to configure one of the plurality of configurable computing matrixes.

348. (New) The method of claim 346, wherein the controller is a RISC controller.

349. (New) The method of claim 339, wherein the first interconnection network operates as a Boolean interconnection network and a data interconnection network, the first interconnection network further allowing the transmission of data and configuration information.

350. (New) The method of claim 349, wherein the matrix interconnection network transmits configuration information to the computing matrix to configure the computing matrix to perform the functions.

351. (New) The method of claim 339, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

352. (New) The method of claim 339, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

353. (New) The method of claim 339, wherein the first plurality of heterogeneous computational elements includes a function generator and an adder, a register and an adder, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the second plurality of heterogeneous computational elements includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

354. (New) The method of claim 353, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

355. (New) The method of claim 354, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

356. (New) The method of claim 339, wherein basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

357. (New) The method of claim 356, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

358. (New) The method of claim 357, wherein the basic computational function comprises bit level manipulation; and

wherein the complex processing function comprises word level manipulation.

359. (New) The method of claim 339, wherein the basic computational function includes one of a group of linear operation, non-linear operation, finite state machine computing, memory, memory management, and bit level manipulation; and

wherein the complex processing function is one of a group of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

360. (New) The method of claim 359, wherein the basic computational function is a logic function; and

wherein the complex processing function is a digital signal processing function.

361. (New) The method of claim 360, wherein the basic computational function comprises it level manipulation; and

wherein the complex processing function comprises word level manipulation.

362. (New) The method of claim 360, wherein the basic computational function includes a function generator and an adder, an adder and a register, a function generator and a register, or a function generator and an adder and a register, the function generator having data inputs and a control input to selection a specific function; and

wherein the complex processing function includes a multiplier and an adder, a multiplier and a register, or a multiplier and an adder and a register.

363. (New) The method of claim 362, wherein the second plurality of heterogeneous computational elements each perform a function from the group of multiplication, addition, subtraction, accumulation, summation, byte passing, and dynamic shift.

364. (New) The method of claim 339, further comprising a third interconnection network coupled to the configurable basic computational unit and the configurable complex computational unit, the third interconnection network sending the configuration information to the units.

365. (New) The method of claim 364, wherein the first interconnection network has denser interconnections than the interconnections of the third interconnection network.

366. (New) The method of claim 339, wherein the first interconnection network includes multiplexers coupled to the first plurality of heterogeneous computational elements.

367. (New) The method of claim 366, wherein the configuration information includes control signals to control the multiplexers.

368. (New) The method of claim 339, wherein the first interconnection network provides a third configuration information to reconfigure the configurable basic computational unit to perform a second computational function, the memory being adapted to store the third configuration information.

REMARKS

In the Notice Of Non-Compliant Amendment mailed on February 20, 2009, the USPTO withdrew all of the claims submitted in the response filed October 14, 2008 as being directed to a non-constructively-elected invention.

In this Amendment, Applicants respectfully submit new claims 182-368 which examination on the merits is respectfully requested. After entry of this Amendmnet, claims 182-368 will be pending.

Conclusion

Applicants respectfully submit that all pending claims, Claims 182-368 the present application are allowable. Such allowance is respectfully solicited.

If a telephone conference would expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (415) 984-8200.

Respectfully submitted,

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May ___, 2009
Dated

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